THE CLAIMS

What is claimed is:

1. A method for manufacturing a semiconductor structure comprising:

providing a predetermined detachment area in a source substrate of a first material;

bonding the source substrate to a handle substrate of a second material to form a source-handle-structure;

annealing the source-handle-structure in multiple annealing steps with a first annealing step conducted at a first energy level which is lower than the energy of a thermal detachment budget, and a second annealing step conducted at a second energy level that is lower than the first energy level to at least prepare at least the source substrate for detachment of a useful layer at the predetermined detachment area in order to obtain a layer of first material supported by handle substrate.

2. The method according to claim 1, wherein the second annealing step is conducted until detachment occurs at the predetermined detachment area to provide the useful layer on the handle substrate.

3. The method according to claim 1, which further comprises detaching the useful layer at the predetermined detachment area by providing additional energy to the source substrate.

4. The method according to claim 3, wherein the additional energy is thermal energy provided by further heating of the source substrate.

5. The method according to claim 3, wherein the additional energy is mechanical energy applied to or near the predetermined detachment area of the source substrate.

6. The method according to claim 1, wherein the first annealing step provides about 70 to 99 % of the energy of the thermal detachment budget.

7. The method according to claim 1, wherein the first annealing step includes heating to a temperature of about 350°C to 500°C for about a few minutes to about a few hours.

8. The method according to claim 7, wherein the second annealing step includes heating to a temperature of about 150°C to 350°C for about a few hours to about a few days, with the temperature of the first annealing step being at least 25% greater than that of the second annealing step, and the second annealing step is conducted for at least twice as long as the first annealing step.

9. The method according to claim 1, wherein annealing at the second energy level includes heating at about 150°C to 350°C for about a few hours to about a few days.

10. The method according to claim 1, further comprising cooling the source-handle-structure between the first and second annealing steps.

11. The method according to claim 10, wherein the source-handle-structure is cooled to a temperature of between about 18°C and 25°C.

12. The method according to claim 10, wherein the source-handle-structure is cooled to the temperature of the second annealing step.

13. The method according to claim 1, wherein the first annealing step includes step-wise heating or cooling to gradually increase or decrease heating temperature.

14. The method according to claim 13, wherein the stepwise heating in the first annealing step increases the time necessary to complete that step but decreases the time necessary to complete the second annealing step.

15. The method according to claim 13, wherein the first annealing step includes heating to a maximum temperature followed by step wise cooling to lower temperatures.

16. The method according to claim 10, wherein the temperature of the first annealing step is cooled to the temperature of the second annealing step.

17. The method according to claim 1, wherein the predetermined detachment area is made by implantation of hydrogen ions, rare gas ions or a combination of hydrogen and rare gas ions to form a zone of weakness that corresponds to the detachment area.

18. The method according to claim 17, wherein the predetermined detachment area is made by implantation of hydrogen ions, helium ions or a combination of hydrogen and helium ions.

19. The method according to claim 1, further comprising cooling the layer of first material and handle structure to room temperature after the second annealing step.

20. The method according to claim 1, wherein the second material of the handle substrate is different from the first material of the source substrate.

21. The method according to claim 1, wherein the first and second materials are at least one of silicon, a group (III)-(V) semiconductor, an alloy of a group (III)-(V) semiconductor, silicon germanium, silicon carbide, synthetic quartz or fused silica.

22. The method according to claim 1, wherein the first and second materials form or comprise a heterogenous semiconductor structure.

23. The method according to claim 22, wherein the source substrate is a silicon wafer and the handle substrate is a wafer of fused silica or synthetic quartz.